REMARKS

The above-referenced patent application has been reviewed in light of the Final Office Action, mailed January 13, 2003, in which: claims 13-15, 18 and 19 are rejected under 35 U.S.C. § 102(b) as being anticipated by Tran, et al. (US-5,780,883) (hereinafter "Tran"), in which claims 16 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran, and in which claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran in view of Farwell (US-5,576,645). Reconsideration of the above-referenced patent application in view of these amendments and remarks is respectfully requested.

Claims 13-20 and 27 are pending in the application. Claims 13 and 18-20 are currently amended. Claims 18-20 have been broadened. Claim 27 is new. Claims 1-12 and 21-26 have been cancelled because they are being prosecuted in the parent application. No prosecution history estoppel results from the cancellation because it merely permits those claims to be prosecuted separately. No claimed subject matter of any kind has been surrendered by these actions.

An informality and minor omission is noted in the specification. This minor error was made inadvertently and without deceptive intent. Appropriate corrections have been made by the foregoing amendments. It is respectfully requested that Examiner approve and enter these minor corrections.

I. REJECTIONS.

(a). Rejection of claims 13-15, 18 and 19 under 35 U.S.C. § 102(b)

Examiner rejected claims 13-15, 18 and 19 under 35 U.S.C. § 102(b) as being anticipated by Tran. Applicant respectfully asserts that Examiner's rejection was in error, that Examiner misapprehends the nature of Applicant's invention and that Tran does not anticipate each and every

element of Applicant's invention. Applicant traverses the rejection of these claims under section 102(b) and respectfully asserts that these claims are in condition for allowance.

Regarding the section 102(b) rejection of claim 13, Applicant noted in Applicant's earlier response, dated October 17, 2002, that Tran fails to disclose partially overlying polysilicon landing sites forming N- and P-type transistors, whereas Applicant claims "diffusion regions having partially overlying polysilicon landing sites to form N-type **and** P-type transistors" (claim 13, emphasis added). Examiner's continuing rejection of this claim under section 102(b) in light of Tran is unfounded.

Applicant respectfully asserts that the polysilicon landings in Tran relied on by Examiner, in Examiner's Office Action dated July 12, 2002, form **either** N- **or** P-type transistors, not both. Looking at, for example, Figure 3A of Tran, it is evident that Tran does not disclose any landings which overlie both an N-diffusion strip **and** a P-diffusion strip. Rather, all of the landings overlie only one diffusion strip. Nowhere in Tran is there a disclosure of a **one** landing overlying **both** an N-diffusion strip **and** a P-diffusion strip. In contrast, Applicant discloses landings overlying both N- and P-diffusion strips, claiming landing sites which form "N-type **and** P-type transistors" (claim 13, emphasis added). Compare, for example, Figure 1 of Applicant's application with Figure 3A of Tran.

Since Tran does not disclose a landing site forming both an N-type and a P-type transistor, Tran does not anticipate this element of Applicant's invention, and since Tran does not anticipate every element of claim 13, Tran is not anticipatory under 35 U.S.C. § 102(b). Thus, Applicant respectfully traverses Examiner's rejection of claim 13 under 35 U.S.C. § 102(b).

Regarding the section 102(b) rejection of claims 14, 15, 18 and 19, Examiner rejected these claims as being anticipated by Tran, yet Examiner failed to offer any justification in any Office Action

for the rejection. Rather, Examiner addressed the elements of claim 13 alone, with no mention of the further elements of claims 14, 15, 18, and 19.

It is well settled Federal Circuit law that a claim is anticipated under 102(b) only if "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP § 2131, citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Examiner appears to be proceeding under the assumption that these dependent claims necessarily stand or fall together with claim 13. However, this is not the case. Rather, 35 U.S.C. § 282 requires "dependent or multiple dependent claims shall be presumed valid even though dependent upon an invalid claim." Thus, when determining the validity of the claims of a patent, each claim must be separately considered. *Rosco, Inc. v. Mirror Lite Co.*, 304 F.3d 1373, 1379 (Fed. Cir. 2002) ("The district court erred by not separately addressing each claim . . . .").

Examiner offered no basis for the rejection of claims 14, 15, 18, and 19 and has not pointed out how Tran is relevant to the elements of these claims. Examiner's reliance on Examiner's challenge to claim 13 is a legally insufficient basis for the rejection of claims 14, 15, 18 and 19. Thus, applicant respectfully traverses Examiner's rejection and asserts that the rejection of claims 14, 15, 18 and 19 under section 102(b) was improper and that these claims are in condition for allowance.

(b). Rejection of claims 16 and 17 under 35 U.S.C. § 103(a)

Examiner rejected claims 16 and 17 under 35 U.S.C. § 103(a) as being unpatentable over Tran, stating that "it would have been within the level of ordinary skill in the art to choose the appropriate ratio between the larger and smaller transistors (or rows) . . . in order to minimize the area and maximize the speed." Applicant respectfully asserts that Examiner failed to establish a *prima facie* case of obviousness under section 103(a) and, therefore, the rejection of these claims on this basis is respectfully traversed, leaving claims 16 and 17 in condition for allowance.

First, it is well settled law that, in order to establish a *prima facie* rejection of claims 16 and 17 under section 103(a), Examiner must demonstrate that each and every element of the claimed invention is present in the cited art. However, Examiner rejected claims 16 and 17 without addressing each and every element in those claims. Claims 16 and 17 are dependent claims which incorporate the elements of claim 15, which in turn incorporates the elements of claim 14. As noted above, Examiner failed to point out any relevance that Tran has to the elements of claims 14 or 15. Thus, it is necessarily follows that Examiner likewise failed to address each and every element of dependent claims 16 and 17. Examiner thereby failed to set forth a *prima facie* case of obviousness by failing to address each and every claim element of claims 16 and 17.

Second, Examiner failed to offer any findings, support or explanation for Examiner's conclusory assertion that the elements of claims 16 and 17 "would have been within the level of ordinary skill in the art." Section 2143 of the Manual of Patent Examining Procedure (hereinafter "MPEP") sets forth the requirements Examiner must satisfy to establish a *prima facie* case of obviousness under section 103(a). One such requirement is that Examiner offer some support for the assertion. By failing to offer support, Examiner thereby commits errors that section 2143 and the Federal Circuit forbid. Section 2143 highlights these errors, citing *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000) ("there was no finding as to the principle or specific understanding within the knowledge of a skilled artisan that would have motivated the skilled artisan to make the claimed invention"). Examiner offered no evidence of the level of ordinary skill in the art, and, as such, has not set forth a *prima facie* case of obviousness under section 103(a).

Third, not only did Examiner fail to set forth a *prima facie* case of obviousness for rejection of claims 16 and 17, the patent cited by Examiner actually teaches away from Applicant's invention. Examiner states in the Office Action: "Tran teaches at column 3, lines 18-25, that size of the

transistors relative to the rows, minimize the area and maximize the speed." Applicant respectfully submits that the cited lines teach away from Applicant's invention because Tran teaches that smaller transistors are not suitable for logic, whereas Applicant implements logic on smaller transistors.

Note that Tran distinguishes transmission gates from logic gates (Tran, column 3, lines 15-17) and also teaches that transmission gates and logic gates have different requirements (Tran, column 3, 18-25). Tran then teaches that larger transistors are required for logic gates such as those used for inverters (Tran, column 3, lines 16-17). This teaches away from Applicant's invention because Applicant discloses implementing inverters on small transistors. Applicant discloses "row[s] of "small transistors . . . which may be used for clock buffering and to create logic gates" (Application of Possley, no. 09/902,907, page 6, lines 5-8 (herein after "Application")). Clock buffers are inverters (Application, page 5, line 14). See also FIG. 5 of the Application, which discloses inverters implemented on the smaller transistors. All told, Tran teaches that larger transistors are required for inverters whereas Applicant does just the opposite by implementing inverters on smaller transistors. Thus, contrary to Examiner's assertion, it would not be obvious to one of ordinary skill in the art to use Tran to choose the appropriate ratio between the larger and smaller transistors, since Tran would teach that small transistors are only useful for transmission gates.

For all of these reasons, Examiner failed to establish a *prima facie* case of obviousness for rejecting claims 16 and 17 under section 103(a). Applicant therefore traverses Examiner's rejection of these claims and respectfully asserts that these claims are in condition for allowance.

(c). Rejection of claim 20 under 35 U.S.C. § 103(a)

Examiner rejected claim 20 under 35 U.S.C. § 103(a) "as being unpatentable over Tran as applied to claim 19 . . . in view of Farwell . . . ." Applicant traverses this rejection. Applicant

respectfully asserts that Examiner failed to state a *prima facie* case of obviousness under section 103(a) and that claim 20 is in condition for allowance.

Examiner failed to state a *prima facie* case of obviousness by failing to address each and every element of claim 20. Claim 20 depends from claim 19, and, as already discussed regarding claim 19, above, Examiner failed to address each and every element of claim 19. To recap, Examiner's rejection of claim 13 under 35 U.S.C. § 102(b), a rejection Applicant respectfully traversed above, did not dispose of the claims depending from claim 13, of which claim 19 is one. Furthermore, Examiner never addressed the limitations of claim 19. As such, the rejection of claim 19 was traversed.

The failure to address each and every element of claim 19 necessarily means that each and every element of claim 20 has not been addressed. Thus, Examiner's assertion that "Trans discloses the claimed invention, except for expressly disclosing clock buffers" is incorrect. Examiner failed to address anything other than the clock buffers, including failing to address all of the limitations of claims 19, 18, 15, and 13. Since Examiner failed to set forth a *prima facie* case of obviousness under section 103(a), Applicant asserts that the rejection of claim 20 was improper, and therefore respectfully traverses Examiner's rejection of claim 20.

In addition, Examiner provided no motivation to combine the Tran and Farwell patents. As discussed above, section 2143 of the MPEP sets forth the requirements Examiner must satisfy to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Section 2143 requires the cited patents to contain a suggestion or motivation to combine them. Examiner failed to make this showing because Examiner does not point out a suggestion or motivation to combine. Instead, Examiner only makes a conclusory statement that "it would have been obvious to one of ordinary skill in the art." In so doing, Examiner has engaged in hindsight speculation that section 2143 and the Federal Circuit

expressly proscribe: "the level of skill in the art cannot be relied upon to provide the suggestion to combine references," (MPEP § 2143, citing *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308 (Fed. Cir. 1999)).

It is noteworthy that section 2143 takes pains to make this point clear, elaborating that "a statement that modifications of the prior art to meet the claimed invention would have been 'well within the ordinary skill of the art at the time the claimed invention was made' because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." (citing *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)) (emphasis added). By repeating the mistakes criticized in section 2143 and failing to show a suggestion or motivation to combine Tran and Farwell, Examiner failed to establish a prima facie case of obviousness under section 103(a).

Finally, Examiner's statement that "it would have been obvious to one of ordinary skill in the art . . . to use clock buffers in order to control the operation of the flip flop" fails to address the element of claim 20 wherein Applicant claims "clock buffers of the flip-flop are formed from the smaller transistors" (emphasis added). Farwell's mere disclosure of internal clock buffers is irrelevant to the sizing of transistors because Farwell says nothing at all about sizing of transistors and thus teaches nothing about placing components of flip-flops on differing size transistors. So, even if one were to combine Tran with Farwell, which Applicant asserts is improper, the combination would fail to teach anything about how to size transistors for clock buffers. Since Farwell teaches nothing about transistor sizing, Examiner's attempt to combine Farwell with Tran is insufficient to render claim 20 obvious under section 103(a).

For all of these reasons, Examiner has failed to establish a *prima facie* case of obviousness for rejecting claim 20 under section 103(a). Applicant therefore traverses Examiner's rejection of this claim and respectfully asserts that it is in condition for allowance.

II. AMENDMENTS TO CLAIMS

Having respectfully traversed all of Examiner's rejections of the claims pending in this application, Applicant nevertheless offers and respectfully requests that Examiner enter the currently amended and new claims. In a related case, application number 09/902,912 (attorney docket number 042390.P6643c), the Examiner in that case made arguments that may be relevant to this application. Applicant respectfully asserts that the claims in this application are in condition for allowance without the current amendments and, as such, respectfully reserves the right to pursue the original claim language on any subsequent appeal. Yet, the current amendments further clarify and distinguish the claims. Therefore, in the interests of advancing prosecution and putting the claims in this application in condition for allowance, Applicant offers the current amendments to the claims.

Claim 13 now specifically recites:

> A method of fabricating an integrated circuit chip comprising:
>
> processing a semiconductor substrate to form a gate array architecture of transistors in the substrate, the gate array architecture comprising a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites ~~to form~~ , at least one forming both N-type and P-type transistors;
>
> wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors.

Applicant respectfully asserts that this amendment further distinguishes claim 13 from the cited patents in at least the respect that Tran does not teach a polysilicon landing site overlying both an N-type and a P-type diffusion region. Therefore, it is respectfully requested that Examiner withdraw all rejections to claim 13 and enter the amended claim.

Claims 14-20 depend from claim 13 and incorporate all the limitations thereof. Since the current amendment to claim 13 further distinguishes it from the cited patents, claims 14-20 are likewise further distinguished from the cited patents. Therefore, it is respectfully requested that Examiner withdraw all rejections to claims 14-20 and enter the amended claims.

Applicant has added claim 27, a new claim. Applicant respectfully asserts that there is adequate support in the specification for this claim. Such support may be found, for example, at lines 16-20 on page 7 and FIG. 5 of the specification.

Claim 27 depends from claim 13 and incorporates all the limitations thereof. In light of Applicant's remarks and arguments regarding the patentability of claim 13, above, and given Applicant's amendments to claim 13, also above, Applicant respectfully asserts that claim 27 further distinguishes from the cited patents and is patentable.

Claim 27 specifically recites:

> The method of claim 13, wherein said transistors are formed in said gate array architecture so that an interconnect disposed thereon is capable of connecting said smaller transistors to form internal clock buffers.

Applicant respectfully asserts that claim 27 is distinguished from the cited patents in at least the respect that Tran teaches that larger transistors are used for clock buffers, inverters and logic gates and Farwell says nothing at all about sizing of transistors, thus teaching nothing about placing components of flip-flops on differing size transistors.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance. Reconsideration of this patent application and early

allowance of all the claims is respectfully requested. If Examiner has any questions Examiner can contact the undersigned at (503) 712-1565 or Howard Skaist at (503) 264-0967.

Respectfully submitted,

Jay Beale
Patent Agent
Reg. No. 50,901

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c/o Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026
(503) 264-0967

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Name of Person Mailing Correspondence

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